CLAIMS

1. A digital transmitting device for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising:
- primary transmitter means for converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels and
- secondary transmitter means for converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

2. A digital transmitting device according to claim 1, comprising means for disabling the output of data signal levels into said output line for the time of outputting synchronization signal levels into said output line.

3. A digital transmitting device according to claim 2, wherein
- said primary transmitter means comprise a first transmitter having a data input, an output and an enable or select input,
- said secondary transmitter means comprise a second transmitter having a data input, an output and an enable or select input,
- the digital transmitting device comprises a selection signal line and
- said selection signal line is coupled to the enable or select input of said first transmitter with direct polarity and to the enable or select input of said second transmitter with reverse polarity.

4. A digital transmitting device according to claim 2, wherein
- said primary transmitter means and said secondary transmitter means are implemented as complementary modes of a single controllable transmitter having a control input to control its amplification factor,
- the digital transmitting device comprises a control signal line and
- said control signal line is coupled to the control input of said single controllable transmitter.

5. A digital transmitting device according to claim 1, comprising means for summing the outputs of said primary transmitter means and said secondary transmitter means into combined output levels in said output line.

6. A digital transmitting device according to claim 1, wherein
- said output line is a differential wired connection consisting of a first signal line and a second signal line, and
- said primary transmitter means is a low-voltage level differential transmitter.

7. A digital transmitting device according to claim 6, wherein said secondary transmitter means is a differential transmitter having differential output levels that are remarkably farther from zero than the output levels of said low-voltage level differential transmitter.

8. A digital transmitting device according to claim 6, wherein said secondary transmitter means comprises a pair of parallel tri-state bus drivers having non-differential output levels that are remarkably farther from zero than the output levels of said low-voltage level differential transmitter.

9. A digital receiving device for receiving a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising:
- primary receiver means, responsive to a first group of signal levels, for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits and
- secondary receiver means, responsive to a second group of signal levels which consists of different levels than said first group of signal levels, for converting synchronization signal levels in said input line into synchronization signals.

10. A digital receiving device according to claim 9, wherein
- said primary receiver means is a low-voltage level differential receiver responsive to voltage signals at a certain first distance from zero,
- said secondary receiver means comprises two parallel differential amplifiers coupled as level indicators to said input line with opposite polarities and responsive to voltage signals at a certain second distance from zero, which is larger than said first distance.

11. A digital receiving device according to claim 10, comprising:
- an enable or select input in said low-voltage level differential receiver and
- a coupling from the outputs of said parallel differential amplifiers to said enable or select input arranged to disable said low-voltage level differential receiver as a

response to an affirmative level indication from either one of said parallel differential amplifiers.

12. A digital receiving device according to claim 10, wherein
- said secondary receiver means comprises also two other parallel differential amplifiers coupled as level indicators to said input line with opposite polarities and responsive to voltage signals at a certain third distance from zero, which is larger than said second distance,
- said four parallel differential amplifiers constitute two differential amplifier pairs so that in each pair the differential amplifiers are coupled as level indicators to said input line with same polarity but responsive to voltage signals at a different distance from zero,
- the digital receiving device comprises additionally inverting means for conditionally inverting the output of said low-voltage level differential receiver as a response to a certain indication and
- from each differential amplifier pair there is a coupling to said inverting means for producing said indication as a response to a situation where exactly one of the amplifiers in the differential amplifier pair gives an affirmative level indication.

13. A digital receiving device according to claim 9, wherein said primary receiver means and said secondary receiver means are implemented within a mapping entity arranged to map a number of input signal levels into corresponding bit combinations where the reception of signal levels belonging to said first group of signal levels corresponds to different bit combinations than the reception of signal levels belonging to said second group of signal levels.

14. A digital receiving device according to claim 13, wherein said mapping entity consists of an analog to digital converter and an associated logic block.

15. An electronic device comprising a first circuit element and a second circuit element for processing digital image data consisting of data sequences and synchronization signals, comprising:
- within the first circuit element a digital transmitting device for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, said digital transmitting device comprising:
    - primary transmitter means for converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels and

- secondary transmitter means for converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels; and

- within the second circuit element a digital receiving device for receiving a serial sequence of data bits and a number of associated synchronization signals over a wired connection, said digital receiving device comprising:

- primary receiver means, responsive to a first group of signal levels, for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits and

- secondary receiver means, responsive to a second group of signal levels which consists of different levels than said first group of signal levels, for converting synchronization signal levels in said input line into synchronization signals.

16. A method for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection, comprising the steps of:

- converting a serial sequence of data bits into successive data signal levels in an output line, said data signal levels being selected from a first group of levels, and

- converting synchronization signals into synchronization signal levels on said output line, said synchronization signal levels being selected from a second group of levels which consists of different levels than said first group of levels.

17. A method according to claim 16, wherein, as a part of the step of converting synchronization signals into synchronization signal levels on said output line, the simultaneous conversion of data bits into successive data signal levels in said output line is disabled so that synchronization signal levels and data signal levels only occur alone in said output line.

18. A method according to claim 16, wherein, as a part of the step of converting synchronization signals into synchronization signal levels on said output line, the simultaneous conversion of data bits into successive data signal levels in said output line is upheld so that synchronization signal levels and data signal levels occur in superposition in said output line.